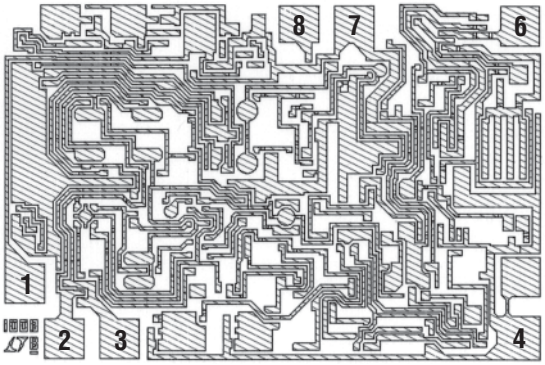

74 × 51 mils

PAD FUNCTION

1. COMP 1
2. –IN
3. +IN
4. V^- (substrate)
5. NC
6. OUT
7. V^+
8. COMP 2

Backside (substrate) is an alloyed gold layer. Connect to V^-.

DIE CROSS REFERENCE (Note 1, 2)

LTC Finished Part Number	Order DICE CANDIDATE Part Number Below
RH108A	RH108A DICE

DICE ELECTRICAL TEST LIMITS (Elemental Evaluation)(Notes 4, 5, 7)

SYMBOL	PARAMETER	CONDITIONS	NOTES	T_A = 25°C MIN	T_A = 25°C MAX	SUB-GROUP	–55°C ≤ T_A ≤ 125°C MIN	–55°C ≤ T_A ≤ 125°C MAX	SUB-GROUP	UNITS
V_{OS}	Input Offset Voltage				0.5	1		1.0	2,3	mV
I_{OS}	Input Offset Current				0.2	1		0.4	2,3	nA
I_B	Input Bias Current				2.0	1		3.0	2,3	nA
A_{VOL}	Large-Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V $R_L \geq 10k$		80		4	40		5,6	V/mV
CMRR	Common Mode Rejection Ratio			96		1	96		2,3	dB
PSRR	Power Supply Rejection Ratio			96		1	96		2,3	dB
	Input Voltage Range	V_S = ±15V	3	±13.5			±13.5			V
V_{OUT}	Output Voltage Swing	V_S = ±15V, R_L = 10k		±13		4	±13		5,6	V
I_S	Supply Current	(Note 6)			0.6	1		0.4 0.6	2 3	mA mA

Note 1: Differential input voltages greater than 1V will cause excessive current to flow through the input diodes unless limiting resistance is used.

Note 2: For supply voltages less than ±15V, the maximum input voltage is equal to the supply voltage.

Note 3: Guaranteed by design, characterization or correlation to other tested parameters.

Note 4: ±5V ≤ V_S ≤ ±20V unless otherwise noted.

Note 5: V_S = ±15V, V_{CM} = 0V, T_A = 25°C unless otherwise noted.

Note 6: 25°C ≤ T_A ≤ 125°C.

Note 7: Dice are probe tested at 25°C to the limits shown. Final specs after assembly are sample tested during the elemental evaluation. Please refer to RH108AH data sheet . For absolute maximum ratings, typical specifications, performance curves and finished product specifications, please refer to the standard RH data sheets.

Rad Hard die require special handling as compared to standard IC chips.

Rad Hard die are susceptible to surface damage because there is no silicon nitride passivation as on standard die. Silicon nitride protects the die surface from scratches by its hard and dense properties. The passivation on Rad Hard die is silicon dioxide that is much “softer” than silicon nitride.

LTC recommends that die handling be performed with extreme care so as to protect the die surface from scratches. If the need arises to move the die around from the chip tray, use a Teflon-tipped vacuum wand. This wand can be made by pushing a small diameter Teflon tubing onto the tip of a steel-tipped wand. The inside diameter of the Teflon tip should match the die size for efficient pickup. The tip of the Teflon should be cut square and flat to ensure good vacuum to die surface. Ensure the Teflon tip remains clean from debris by inspecting under stereoscope.

During die attach, care must be exercised to ensure no tweezers touch the top of the die.

Wafer level testing is performed per the indicated specifications for dice. Considerable differences in performance can often be observed for dice versus packaged units due to the influences of packaging and assembly on certain devices and/or parameters. Please consult factory for more information on dice performance and lot qualifications via lot sampling test procedures.

Dice data sheet subject to change. Please consult factory for current revision in production.

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408)432-1900 • FAX: (408) 434-0507 • www.linear-tech.com

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